REMARKS

In the Final Office Action, the Examiner noted that claims 1 and 21-39 are pending in the application and that claims 1 and 21-39 are rejected. By this response, claim 1 is amended. In view of the above amendments and the following discussion, Applicants submit that all of the claims now pending in the application satisfy 35 U.S.C. §112, first paragraph, and that none of such claims are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims Under 35 U.S.C. §112

The Examiner rejected claims 1 and 21-39 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner stated that the following limitations lack written support in the specification: (1) obtaining a target architecture; (2) generating an intermediate representation from the RDL description; (3) traversing the intermediate representation to produce a program language file; and (4) invoking the program language file using a high-level synthesis compiler to generate a graph of the target architecture. (Final Office Action, p. 2). The rejection is respectfully traversed.

The step of "obtaining a target architecture" in claim 1 is supported by the specification at least on page 7, line 2 (stating that "[t]he architecture of the target is presented as an input (Block 1)"). Applicants have amended claim 1 to recite that an "intermediate graph representation" is generated from the RDL description. The step of "generating an intermediate graph representation from the RDL description" in claim 1 is supported by the specification at least on page 7, lines 7-9 (stating that "[b]lock 2 takes in as input a single RDL description of the target architecture and creates an intermediate graph representation of the architecture so as to perform optimizations").

Applicants have also amended claim 1 to delete reference to the "program language file." The step of "traversing the intermediate graph representation" in claim 1 is supported by the specification at least on page 7, lines 24-25 (stating that "[o]nce the RDL file is parsed and stored in an intermediate AST, the RDL graph creation pass traverses the RDL AST"). The step of "invoking results of the traversing step using a

high-level synthesis compiler to generate a functionality graph and resource graphs for the target architecture" in claim 1 is supported by the specification at least on page 7, lines 24-26 (stating that "the RDL graph creation pass traverses the RDL AST and outputs a C++ file, which when invoked by a high-level synthesis compiler, returns a graph of the target architecture"). See also, Applicants' specification, p. 8, lines 4-6, which states that "[c]ompilation and synthesis of an application entails generation of resource graphs and functionality graph."

Accordingly, each of the features in claim 1 cited by the Examiner has direct and explicit support in the specification. The Examiner did not provide any specific rationale for rejecting claims 21-39, other than their dependency from rejected independent claim 1. Therefore, Applicants contend that claims 1 and 21-39 fully satisfy the written description requirement of 35 U.S.C. §112, first paragraph. Applicants respectfully request that the present rejection of such claims be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1 and 21-39 as being anticipated by Bowen (U.S. Published Patent Application 2003/0105620, published June 5, 2003). The rejection is respectfully traversed.

Bowen generally teaches writing first computer code in a first programming language (e.g., Handel-C), where the first computer code references second computer code in a second programming language (e.g., EDIF, VHDL). The second computer code is simulated for use during the execution of the first computer code in the first programming language. (See Bowen, Abstract; Claims 1-20). The Examiner specifically cites paragraph 0145 of Bowen, which generally describes the use of Handel-C to program FPGAs. The Examiner also cites paragraph 0268 of Bowen, which states that a compiler processes Handel-C code to produce a file, which in turn is compiled into native PC code using Microsoft Visual C++.

Bowen, however, does not teach each and every element of Applicants' invention recited in claim 1. The Examiner is equating three steps described in Bowen to four steps of Applicants' claim 1. Namely, the Examiner equates: (1) creating an Handel-C file in Bowen with construction of an RDL description in Applicants' claim 1;

(2) creating a file at a compiler in Bowen with generating an intermediate representation from the RDL description in Applicants' claim 1; and (3) compiling the file with Microsoft Visual C++ in Bowen with both steps of traversing an intermediate representation and invoking the results of the traversal using a compiler to generate graphs for the target architecture in Applicants' claim 1. Compiling a file with Microsoft Visual C++, however, does not teach or suggest both traversing an intermediate representation of the RDL description and invoking the results of the traversal using a compiler to generate graphs for the target architecture. At best, compiling a file with Microsoft Visual C++ might arguably teach traversing a file. There is, however, no teaching or suggestion in Bowen that the Microsoft Visual C++ compiler generates graphs for the target architecture.

In particular, Applicants have amended claim 1 to recite that a functionality graph and resource graphs are generated by the high-level synthesis compiler. As recited in Applicants' specification, in an embodiment, resource graphs represent the available resources and their capabilities. In an embodiment, the functionality graph represents the graph of the required functionality from the application. (Applicants' specification, p. 8, lines 4-10). Bowen is devoid of any teaching or suggestion of invoking results of the traversal using a high-level synthesis compiler to generate a functionality graph and resource graphs for the target architecture, as recited in Applicants' claim 1. Note that Figures 62-76 of Bowen show timing diagrams for circuits specified in Handel-C. While one may refer to these timing diagrams as "graphs," they are not graphs generated by a high-level synthesis compiler. Bowen does not teach or suggest that the Microsoft Visual C++ compiler generates the timing diagrams.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Bowen does not teach invoking the results of the traversal using a compiler to generate a functionality graph and resource graphs for the target architecture. Thus, Bowen does not teach each and every element of Applicants' amended claim 1 as arranged therein.

Claims 21-39 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since Bowen does not anticipate Applicants' invention as recited in claim 1, dependent claims 21-39 are also not anticipated and are allowable. Accordingly, Applicants contend that claims 1 and 21-39 are not anticipated by Bowen and, as such, fully satisfy the requirements of 35 U.S.C. §102. Applicants respectfully request that the present rejection of such claims be withdrawn.

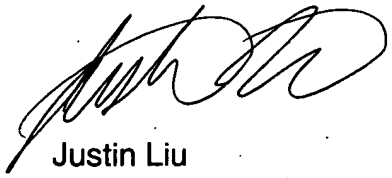
CONCLUSION

Thus, Applicants submit that each of the claims presently in the application satisfy the written description requirement of 35 U.S.C. §112, first paragraph, and that none of such claims are anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Justin Liu at (408) 879-4641 so appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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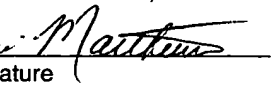
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 13, 2006.

Julie Matthews
Name



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